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Energy Metering IC with Pulse Output

ADE7755*

FEATURES

- High Accuracy, Surpasses 50 Hz/60 Hz IEC 687/1036
- Less than 0.1% Error over a Dynamic Range of 500 to 1
- The ADE7755 Supplies *Average Real Power* on the Frequency Outputs F1 and F2
- The High-Frequency Output CF Is Intended for Calibration and Supplies *Instantaneous Real Power*
- Pin Compatible with AD7755 with Synchronous CF and F1/F2 Outputs
- The Logic Output REVP Can Be Used to Indicate a Potential Miswiring or Negative Power
- Direct Drive for Electromechanical Counters and Two Phase Stepper Motors (F1 and F2)
- A PGA in the Current Channel Allows the Use of Small Values of *Shunt* and *Burden* Resistance
- Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
- On-Chip Power Supply Monitoring
- On-Chip Creep Protection (No Load Threshold)
- On-Chip Reference 2.5 V ± 8% (30 ppm/°C Typical) with External Overdrive Capability
- Single 5 V Supply, Low Power (15 mW Typical)
- Low Cost CMOS Process

GENERAL DESCRIPTION

The ADE7755 is pin compatible with the AD7755. The only difference between the ADE7755 and the AD7755 is that the ADE7755 features a synchronous CF and F1/F2 outputs under all load conditions.

The ADE7755 is a high accuracy electrical energy measurement IC. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard. See Analog Devices' Application Note AN-559 for a description of an IEC1036 watt-hour meter reference design based on the AD7755.

The only analog circuitry used in the ADE7755 is in the ADCs and reference circuit. All other signal processing (e.g., multiplication and filtering) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

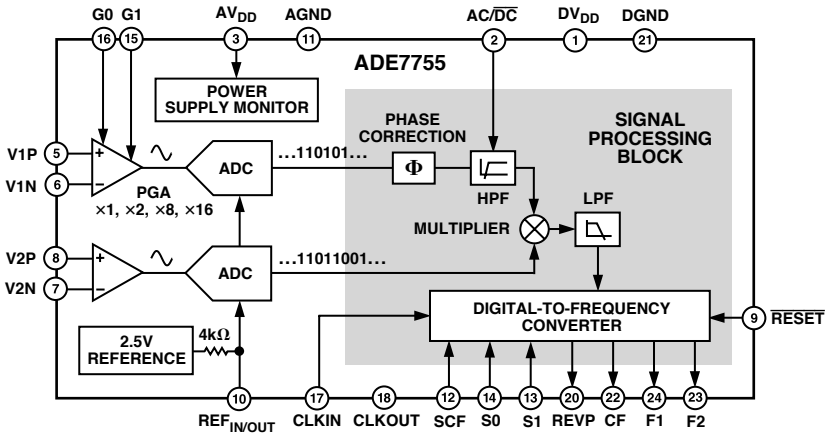
The ADE7755 supplies average real power information on the low-frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or interface to an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes or for interfacing to an MCU.

The ADE7755 includes a power supply monitoring circuit on the AV_{DD} supply pin. The ADE7755 will remain in a reset condition until the supply voltage on AV_{DD} reaches 4 V. If the supply falls below 4 V, the ADE7755 will also be reset and no pulses will be issued on F1, F2, and CF.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched whether the HPF in Channel 1 is on or off. An internal no-load threshold ensures that the ADE7755 does not exhibit any creep when there is no load.

The ADE7755 is available in a 24-lead SSOP package.

FUNCTIONAL BLOCK DIAGRAM



*U.S. Patents 5,745,323, 5,760,617, 5,862,069, and 5,872,469.

REV. 0

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ADE7755—SPECIFICATIONS (AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = –40°C to +85°C.)

Parameter	Specifications	Unit	Test Conditions/Comments
ACCURACY[1, 2]			
Measurement Error[1] on Channel 1			Channel 2 with Full-Scale Signal (±660 mV), 25°C
Gain = 1	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Gain = 2	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Gain = 8	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Gain = 16	0.1	% Reading typ	Over a Dynamic Range 500 to 1
Phase Error[1] Between Channels			Line Frequency = 45 Hz to 65 Hz
V1 Phase Lead 37°			
(PF = 0.8 Capacitive)	±0.1	Degrees(°) max	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
V1 Phase Lag 60°			
(PF = 0.5 Inductive)	±0.1	Degrees(°) max	AC/$\overline{DC}$ = 0 and AC/$\overline{DC}$ = 1
AC Power Supply Rejection[1]			AC/$\overline{DC}$ = 1, S0 = S1 = 1, G0 = G1 = 0
Output Frequency Variation (CF)	0.2	% Reading typ	V1 = 100 mV rms, V2 = 100 mV rms, @ 50 Hz Ripple on AV_{DD} of 200 mV rms @ 100 Hz
DC Power Supply Rejection[1]			AC/$\overline{DC}$ = 1, S0 = S1 = 1, G0 = G1 = 0
Output Frequency Variation (CF)	±0.3	% Reading typ	V1 = 100 mV rms, V2 = 100 mV rms, AV_{DD} = DV_{DD} = 5 V ± 250 mV
ANALOG INPUTS			See Analog Inputs section
Maximum Signal Levels	±1	V max	V1P, V1N, V2N, and V2P to AGND
Input Impedance (DC)	390	kΩ min	CLKIN = 3.58 MHz
Bandwidth (–3 dB)	14	kHz typ	CLKIN/256, CLKIN = 3.58 MHz
ADC Offset Error[1, 2]	±25	mV max	Gain = 1, See Terminology and Performance Graphs
Gain Error[1]	±7	% Ideal typ	External 2.5 V Reference, Gain = 1 V1 = 470 mV dc, V2 = 660 mV dc
Gain Error Match[1]	±0.2	% Ideal typ	External 2.5 V Reference
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.7	V max	2.5 V + 8%
	2.3	V min	2.5 V – 8%
Input Impedance	3.2	kΩ min	
Input Capacitance	10	pF max	
ON-CHIP REFERENCE			Nominal 2.5 V
Reference Error	±200	mV max	
Temperature Coefficient	±30	ppm/°C typ	
CLKIN			Note All Specifications for CLKIN of 3.58 MHz
Input Clock Frequency	4	MHz max	
	1	MHz min	
LOGIC INPUTS[3]			
SCF, S0, S1, AC/$\overline{DC}$, $\overline{RESET}$, G0, and G1			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD} = 5 V ± 5%
Input Current, I_{IN}	±3	μA max	Typically 10 nA, V_{IN} = 0 V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS[3]			
F1 and F2			
Output High Voltage, V_{OH}			I_{SOURCE} = 10 mA
	4.5	V min	DV_{DD} = 5 V
Output Low Voltage, V_{OL}			I_{SINK} = 10 mA
	0.5	V max	DV_{DD} = 5 V
CF and REVP			
Output High Voltage, V_{OH}			I_{SOURCE} = 5 mA
	4	V min	DV_{DD} = 5 V
Output Low Voltage, V_{OL}			I_{SINK} = 5 mA
	0.5	V max	DV_{DD} = 5 V

Parameter	Specifications	Unit	Test Conditions/Comments
POWER SUPPLY			For Specified Performance
AV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
DV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
AI_{DD}	3	mA max	Typically 2 mA
DI_{DD}	2.5	mA max	Typically 1.5 mA

NOTES
[1]See Terminology section for explanation of specifications.
[2]See Plots in Typical Performance Graphs.
[3]Sample tested during initial release and after any redesign or process change that may affect this parameter.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2] (AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 3.58 MHz, T_{MIN} to T_{MAX} = –40°C to +85°C.)

Parameter	Specifications	Unit	Test Conditions/Comments
t_1[3]	275	ms	F1 and F2 Pulsewidth (Logic Low)
t_2	See Table III	sec	Output Pulse Period. See Transfer Function section.
t_3	1/2 t_2	sec	Time between F1 Falling Edge and F2 Falling Edge
t_4[3, 4]	90	ms	CF Pulsewidth (Logic High)
t_5	See Table IV	sec	CF Pulse Period. See Transfer Function section.
t_6	CLKIN/4	sec	Minimum Time between F1 and F2 Pulse

NOTES
[1]Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2]See Figure 1.
[3]The pulsewidths of F1, F2, and CF are not fixed for higher output frequencies. See Frequency Outputs section.
[4]The CF pulse is always 18 µs in the high-frequency mode. See Frequency Outputs section and Table IV.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*
(T_A = 25°C unless otherwise noted.)

AV_{DD} to AGND . . . . . –0.3 V to +7 V
DV_{DD} to DGND . . . . . –0.3 V to +7 V
DV_{DD} to AV_{DD} . . . . . –0.3 V to +0.3 V
Analog Input Voltage to AGND
V1P, V1N, V2P, and V2N . . . . . –6 V to +6 V
Reference Input Voltage to AGND . . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND . . . –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND . . –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Industrial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
24-Lead SSOP, Power Dissipation . . . . . 450 mW
θ_{JA} Thermal Impedance . . . . . 112°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Package Description	Package Options
ADE7755ARS	Shrink Small Outline Package	RS-24
ADE7755ARSRL	Shrink Small Outline Package in Reel	RSRL-24
ADE7755AN-REF	ADE7755 Reference Design PCB (See AN-559)	
EVAL-ADE7755EB	ADE7755 Evaluation Board	

CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7755 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

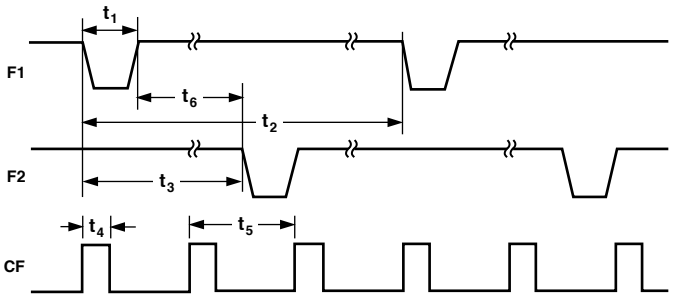
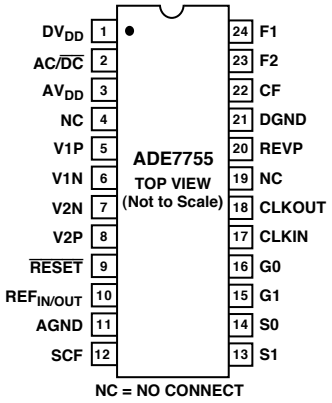


Figure 1. Timing Diagram for Frequency Outputs

PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DV_{DD}	Digital Power Supply. This pin provides the supply voltage for the digital circuitry in the ADE7755. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
2	AC/$\overline{DC}$	High-Pass Filter Select. This logic input is used to enable the HPF in Channel 1 (Current Channel). A logic one on this pin enables the HPF. The associated phase response of this filter has been internally compensated over a frequency range of 45 Hz to 1 kHz. The HPF filter should be enabled in power metering applications.
3	AV_{DD}	Analog Power Supply. This pin provides the supply voltage for the analog circuitry in the ADE7755. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin by the use of proper decoupling. This pin should be decoupled to AGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
4, 19	NC	No Connect
5, 6	V1P, V1N	Analog Inputs for Channel 1 (Current Channel). These inputs are fully differential voltage inputs with a maximum differential signal level of ±470 mV for specified operation. Channel 1 also has a PGA, and the gain selections are outlined in Table I. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry. An overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
7, 8	V2N, V2P	Negative and Positive Inputs for Channel 2 (Voltage Channel). These inputs provide a fully differential input pair. The maximum differential input voltage is ±660 mV for specified operation. The maximum signal level at these pins is ±1 V with respect to AGND. Both inputs have internal ESD protection circuitry, and an overvoltage of ±6 V can also be sustained on these inputs without risk of permanent damage.
9	$\overline{RESET}$	Reset Pin for the ADE7755. A logic low on this pin will hold the ADCs and digital circuitry in a reset condition. Bringing this pin logic low will clear the ADE7755 internal registers.
10	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 µF ceramic capacitor and 100 nF ceramic capacitor.
11	AGND	This provides the ground reference for the analog circuitry in the ADE7755, i.e., ADCs and reference. This pin should be tied to the analog ground plane of the PCB. The analog ground plane is the ground reference for all analog circuitry, e.g., antialiasing filters and current and voltage transducers. For good noise suppression, the analog ground plane should only connect to the digital ground plane at one point. A star ground configuration will help to keep noisy digital currents away from the analog circuits.
12	SCF	Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table IV shows how the calibration frequencies are selected.
13, 14	S1, S0	These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See Selecting a Frequency for an Energy Meter Application section.
15, 16	G1, G0	These logic inputs are used to select one of four possible gains for Channel 1, i.e., V1. The possible gains are 1, 2, 8, and 16. See Analog Input section.
17	CLKIN	An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7755. The clock frequency for specified operation is 3.579545 MHz. Crystal load capacitance of between 22 pF and 33 pF (ceramic) should be used with the gate oscillator circuit.
18	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7755. The CLKOUT Pin can drive one CMOS load when an external clock is supplied at CLKIN or by the gate oscillator circuit.
20	REVP	This logic output will go logic high when negative power is detected, i.e., when the phase angle between the voltage and current signals is greater than 90°. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time as a pulse is issued on CF.

Pin No.	Mnemonic	Description
21	DGND	This provides the ground reference for the digital circuitry in the ADE7755, i.e., multiplier, filters, and digital-to-frequency converter. This pin should be tied to the digital ground plane of the PCB. The digital ground plane is the ground reference for all digital circuitry, e.g., counters (mechanical and digital), MCUs, and indicator LEDs. For good noise suppression, the analog ground plane should only be connected to the digital ground plane at one point only, e.g., a star ground.
22	CF	Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. Also see SCF Pin description.
23, 24	F2, F1	Low Frequency Logic Outputs. F1 and F2 supply *average real power* information. The logic outputs can be used to directly drive electromechanical counters and two phase stepper motors. See Transfer Function section.

TERMINOLOGY

MEASUREMENT ERROR

The error associated with the energy measurement made by the ADE7755 is defined by the following formula:

$$Percentage\ Error = \frac{Energy\ Registered\ by\ the\ ADE7755 - True\ Energy}{True\ Energy} \times 100\%$$

PHASE ERROR BETWEEN CHANNELS

The HPF (High-Pass Filter) in Channel 1 has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is also placed in Channel 1. The phase correction network matches the phase to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range 40 Hz to 1 kHz. See Figures 4 and 5.

POWER SUPPLY REJECTION

This quantifies the ADE7755 measurement error as a percentage of the reading when the power supplies are varied.

For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supplies and a second reading obtained under the same input signal levels. Any error introduced is expressed as a percentage of the reading (see Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. The supplies are then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of the reading.

ADC OFFSET ERROR

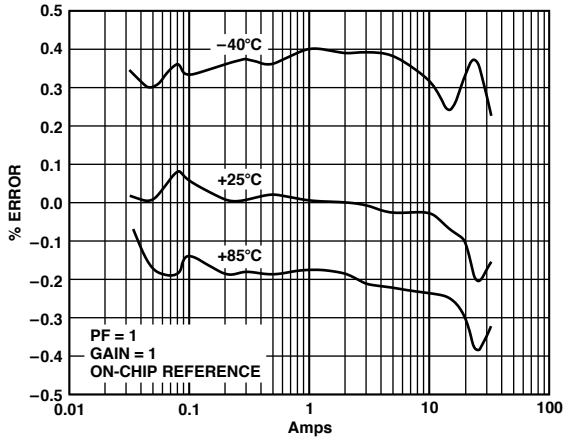
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a small dc signal (offset). The offset decreases with increasing gain in Channel V1. This specification is measured at a gain of 1. At a gain of 16, the dc offset is typically less than 1 mV. However, when the HPF is switched on, the offset is removed from the current channel and the power calculation is not affected by this offset.

GAIN ERROR

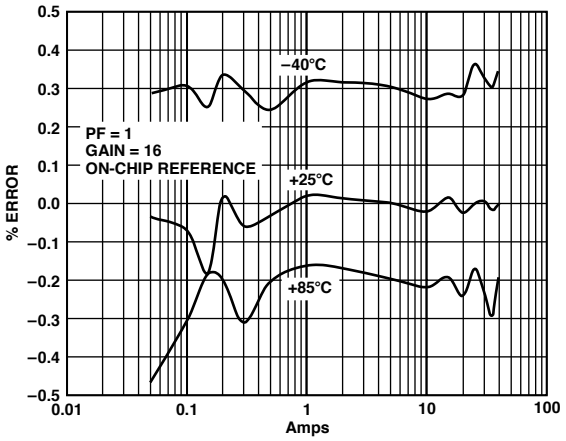
The gain error of the ADE7755 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. It is measured with a gain of 1 in Channel V1. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7755 transfer function (see Transfer Function section).

GAIN ERROR MATCH

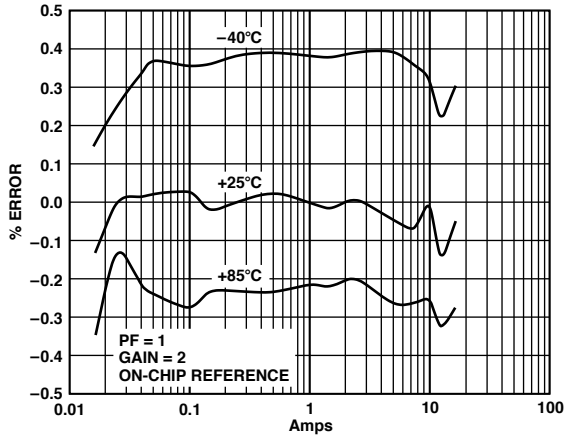
The gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1 and a gain of 2, 8, or 16. It is expressed as a percentage of the output frequency obtained under a gain of 1. This gives the gain error observed when the gain selection is changed from 1 to 2, 8, or 16.



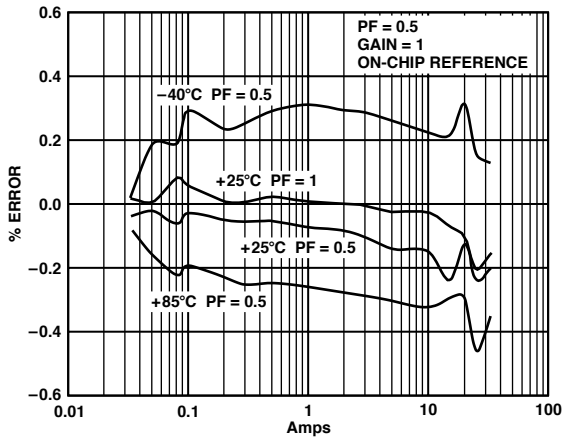
TPC 1. Error as a % of Reading (Gain = 1)



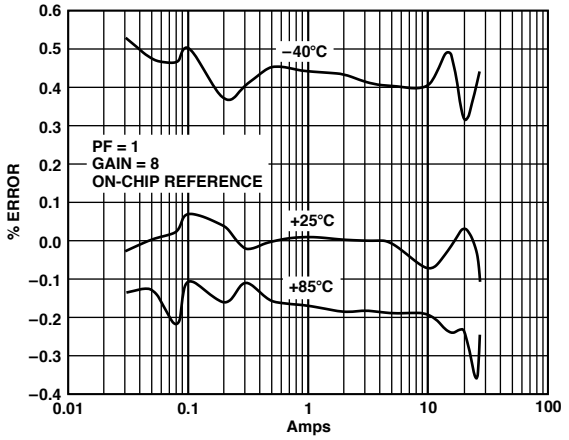
TPC 4. Error as a % of Reading (Gain = 16)



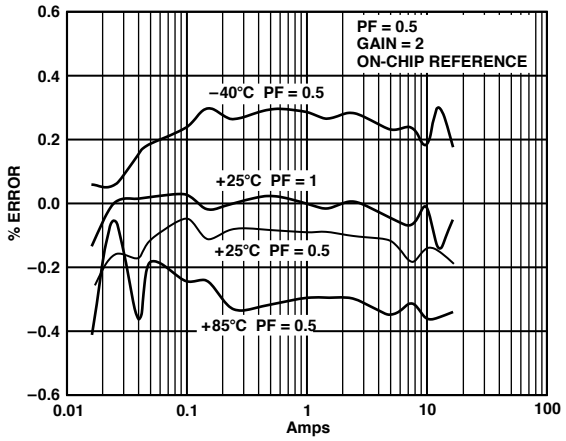
TPC 2. Error as a % of Reading (Gain = 2)



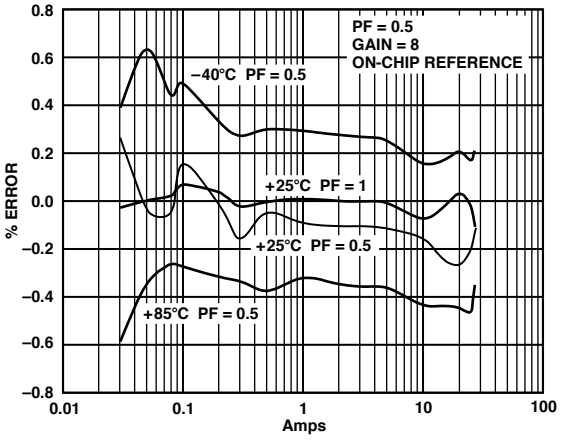
TPC 5. Error as a % of Reading (Gain = 1)



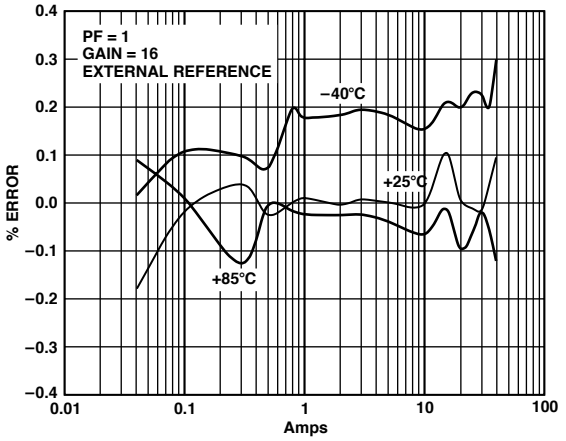
TPC 3. Error as a % of Reading (Gain = 8)



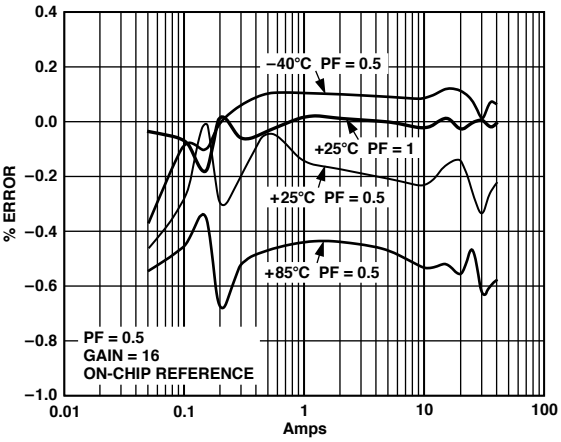
TPC 6. Error as a % of Reading (Gain = 2)



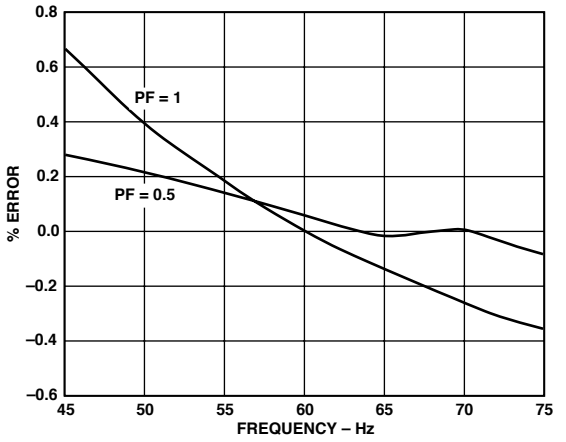
TPC 7. Error as a % of Reading (Gain = 8)



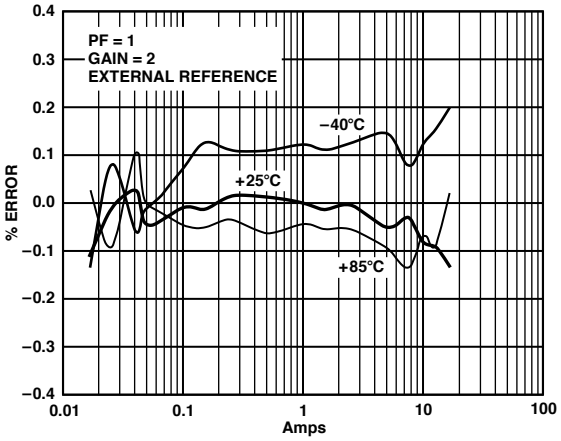
TPC 10. Error as a % of Reading over Temperature with an External Reference (Gain = 16)



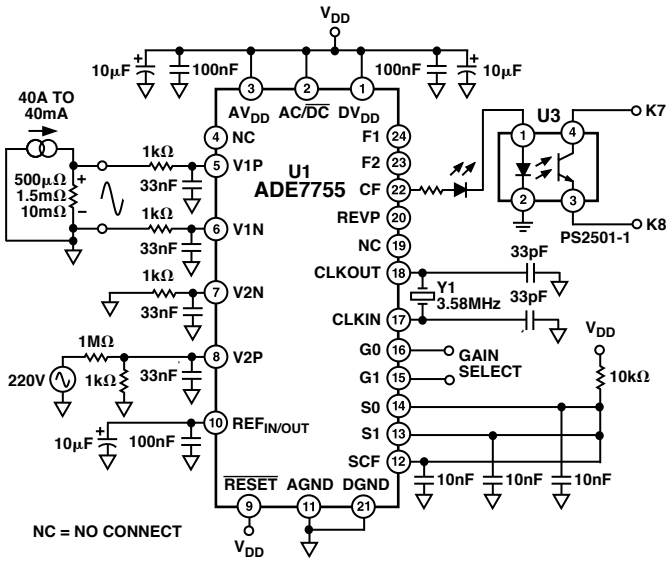
TPC 8. Error as a % of Reading (Gain = 16)



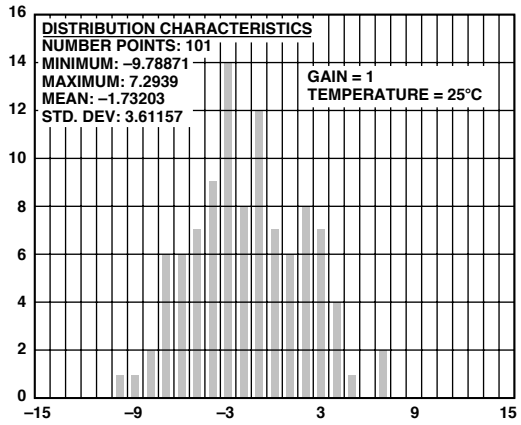
TPC 11. Error as a % of Reading over Frequency



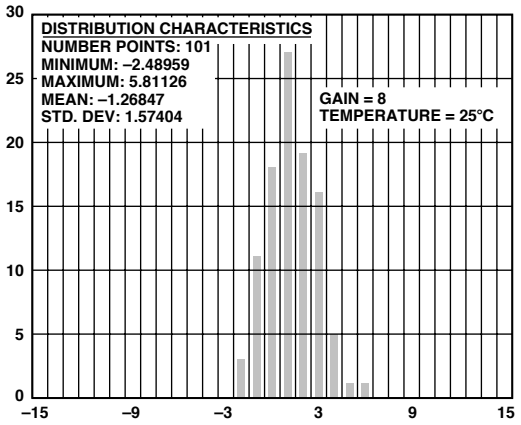
TPC 9. Error as a % of Reading over Temperature with an External Reference (Gain = 2)



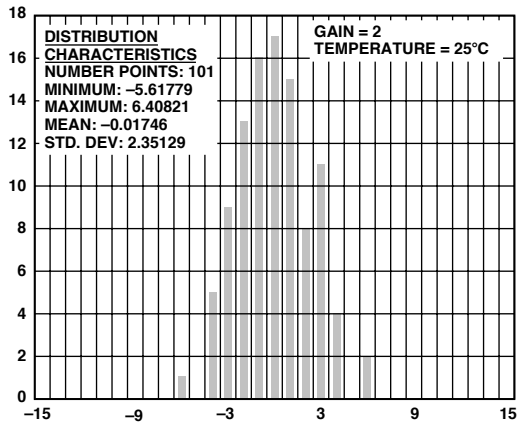
TPC 12. Test Circuit for Performance Curves



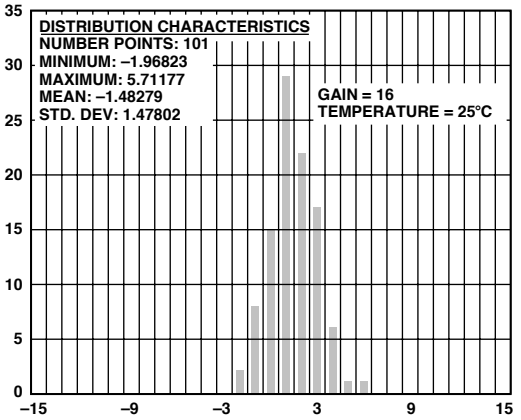
TPC 13. Channel 1 Offset Distribution (Gain = 1)



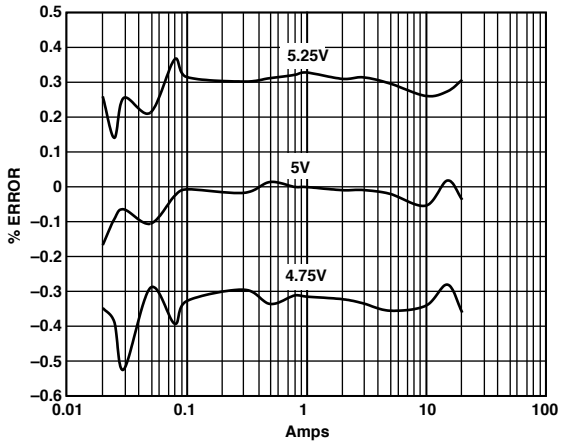
TPC 16. Channel 1 Offset Distribution (Gain = 8)



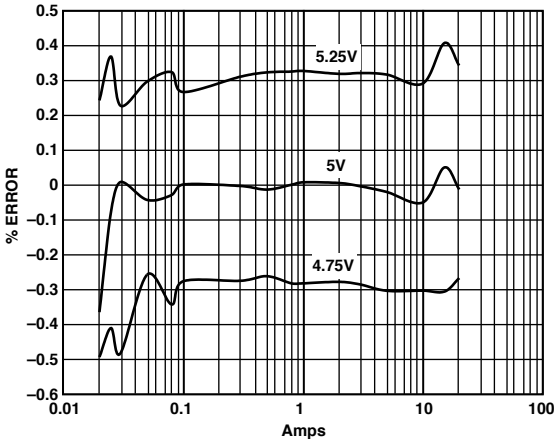
TPC 14. Channel 1 Offset Distribution (Gain = 2)



TPC 17. Channel 1 Offset Distribution (Gain = 16)



TPC 15. PSR with Internal Reference (Gain = 16)



TPC 18. PSR with External Reference (Gain = 16)

THEORY OF OPERATION

The two ADCs digitize the voltage signals from the current and voltage transducers. These ADCs are 16-bit second order sigma-delta with an oversampling rate of 900 kHz. This analog input structure greatly simplifies transducer interfacing by providing a wide dynamic range for direct connection to the transducer and also by simplifying the antialiasing filter design. A programmable gain stage in the current channel further facilitates easy transducer interfacing. A high-pass filter in the current channel removes any dc component from the current signal. This eliminates any inaccuracies in the real power calculation due to offsets in the voltage or current signals (see HPF and Offset Effects section).

The real power calculation is derived from the instantaneous power signal. The instantaneous power signal is generated by a direct multiplication of the current and voltage signals. In order to extract the real power component (i.e., the dc component), the instantaneous power signal is low-pass filtered. Figure 2 illustrates the instantaneous real power signal and shows how the real power information can be extracted by low-pass filtering the instantaneous power signal. This scheme correctly calculates real power for nonsinusoidal current and voltage waveforms at all power factors. All signal processing is carried out in the digital domain for superior stability over temperature and time.

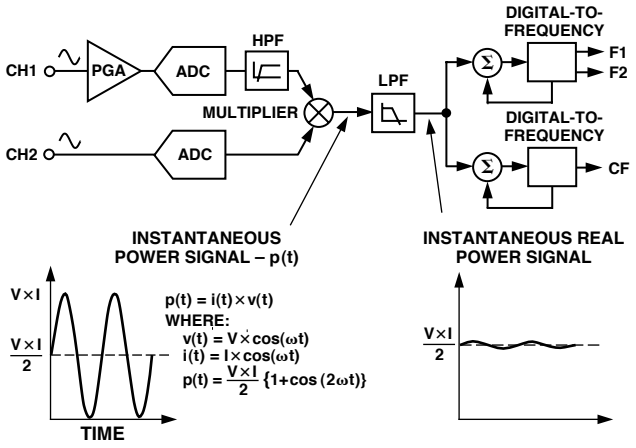


Figure 2. Signal Processing Block Diagram

The low-frequency output of the ADE7755 is generated by accumulating this real power information. This low frequency inherently means a long accumulation time between output pulses. The output frequency is therefore proportional to the average real power. This average real power information can, in turn, be accumulated (e.g., by a counter) to generate real energy information. Because of its high output frequency and shorter integration time, the CF output is proportional to the instantaneous real power. This is useful for system calibration purposes that would take place under steady load conditions.

Power Factor Considerations

The method used to extract the real power information from the instantaneous power signal (i.e., by low-pass filtering) is still valid even when the voltage and current signals are not in phase. Figure 3 displays the unity power factor condition and a DPF (Displacement Power Factor) = 0.5, i.e., current signal lagging the voltage by 60°. If we assume the voltage and current waveforms are sinusoidal, the real power component of the instantaneous power signal (i.e., the dc term) is given by:

$$\left(\frac{V \times I}{2}\right) \times \cos\left(60^{\circ}\right)$$

This is the correct real power calculation.

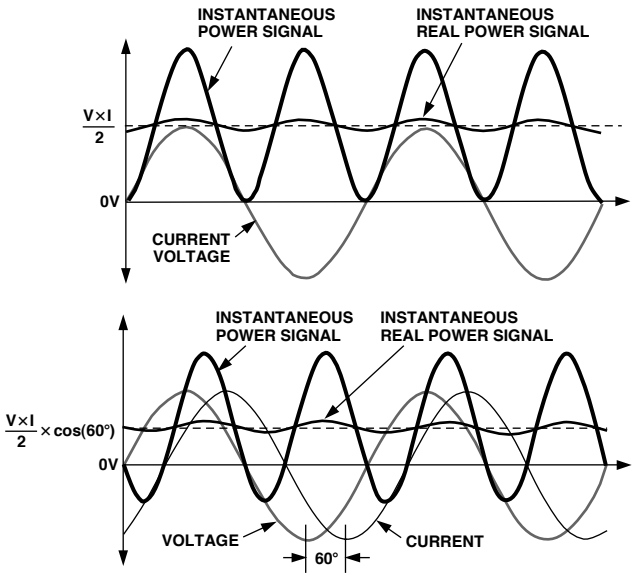


Figure 3. DC Component of Instantaneous Power Signal Conveys Real Power Information PF < 1

Nonsinusoidal Voltage and Current

The real power calculation method also holds true for nonsinusoidal current and voltage waveforms. All voltage and current waveforms in practical applications will have some harmonic content. Using the Fourier Transform, instantaneous voltage and current waveforms can be expressed in terms of their harmonic content.

$$v(t) = V_O + \sqrt{2} \times \sum_{h \neq 0}^{\infty} Vh \times \sin(h\omega t + \alpha h) \quad (1)$$

where:

$v(t)$ is the instantaneous voltage
V_O is the average value
Vh is the rms value of voltage harmonic h
and
αh is the phase angle of the voltage harmonic

$$i(t) = I_O + \sqrt{2} \times \sum_{h \neq 0}^{\infty} Ih \times \sin(h\omega t + \beta h) \quad (2)$$

where:

$i(t)$ is the instantaneous current
I_O is the dc component
Ih is the rms value of current harmonic h
and
βh is the phase angle of the current harmonic

Using Equations 1 and 2, the real power P can be expressed in terms of its fundamental real power (P_1) and harmonic real power (P_H).

$$P = P_1 + P_H$$

where:

$$P_1 = V_1 \times I_1 \cos \phi_1$$
$$\phi_1 = \alpha_1 - \beta_1 \quad (3)$$

and:

$$P_H = \sum_{h \neq 1}^{\infty} Vh \times Ih \cos \phi h$$
$$\phi h = \alpha h - \beta h \quad (4)$$

As can be seen from Equation 4 above, a harmonic real power component is generated for every harmonic, provided that harmonic is present in both the voltage and current waveforms. The power factor calculation has previously been shown to be accurate in the case of a pure sinusoid; therefore the harmonic real power must also correctly account for the power factor since it is made up of a series of pure sinusoids.

Note that the input bandwidth of the analog inputs is 14 kHz with a master clock frequency of 3.5795 MHz.

ANALOG INPUTS

Channel V1 (Current Channel)

The voltage output from the current transducer is connected to the ADE7755 here. Channel V1 is a fully differential voltage input. V1P is the positive input with respect to V1N.

The maximum peak differential signal on Channel 1 should be less than ±470 mV (330 mV rms for a pure sinusoidal signal) for specified operation. Note that Channel 1 has a programmable gain amplifier (PGA) with user selectable gain of 1, 2, 8, or 16 (see Table I). These gains facilitate easy transducer interfacing.

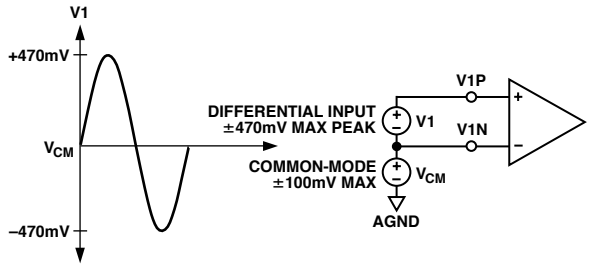


Figure 4. Maximum Signal Levels, Channel 1, Gain = 1

The diagram in Figure 4 illustrates the maximum signal levels on V1P and V1N. The maximum differential voltage is ±470 mV divided by the gain selection. The differential voltage signal on the inputs must be referenced to a common mode, e.g., AGND. The maximum common-mode signal is ±100 mV as shown in Figure 4.

Table I. Gain Selection for Channel 1

G1	G0	Gain	Maximum Differential Signal
0	0	1	±470 mV
0	1	2	±235 mV
1	0	8	±60 mV
1	1	16	±30 mV

Channel V2 (Voltage Channel)

The output of the line voltage transducer is connected to the ADE7755 at this analog input. Channel V2 is a fully differential voltage input. The maximum peak differential signal on Channel 2 is ±660 mV. Figure 5 illustrates the maximum signal levels that can be connected to the ADE7755 Channel 2.

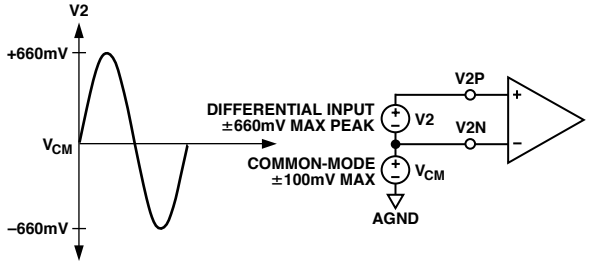


Figure 5. Maximum Signal Levels, Channel 2

Channel 2 must be driven from a common-mode voltage, i.e., the differential voltage signal on the input must be referenced to a common mode (usually AGND). The analog inputs of the ADE7755 can be driven with common-mode voltages of up to 100 mV with respect to AGND. However, best results are achieved using a common mode equal to AGND.

Typical Connection Diagrams

Figure 6 shows a typical connection diagram for Channel V1. A CT (current transformer) is the current transducer selected for this example. Notice the common-mode voltage for Channel 1 is AGND and is derived by center tapping the burden resistor to AGND. This provides the complementary analog input signals for V1P and V1N. The CT turns ratio and burden resistor Rb are selected to give a peak differential voltage of ±470 mV/Gain at maximum load.

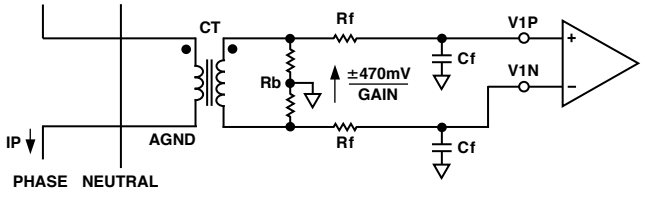


Figure 6. Typical Connection for Channel 1

Figure 7 shows two typical connections for Channel V2. The first option uses a PT (potential transformer) to provide complete isolation from the power line. In the second option, the ADE7755 is biased around the neutral wire, and a resistor divider provides a voltage signal that is proportional to the line voltage. Adjusting the ratio of Ra, Rb, and VR is also a convenient way of carrying out a gain calibration on the meter.

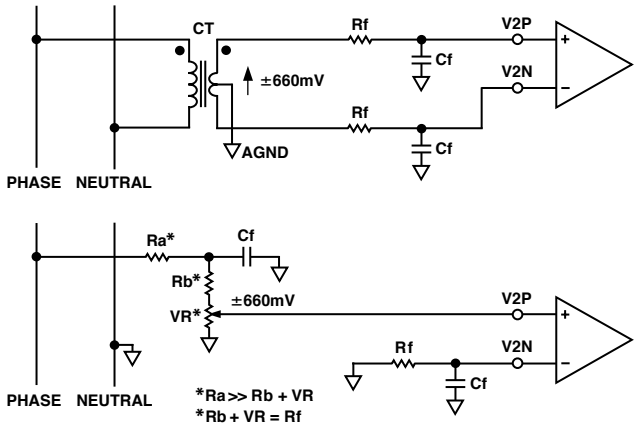


Figure 7. Typical Connections for Channel 2

POWER SUPPLY MONITOR

The ADE7755 contains an on-chip power supply monitor. The Analog Supply (AV_{DD}) is continuously monitored by the ADE7755. If the supply is less than 4 V ± 5%, the ADE7755 will be reset. This is useful to ensure correct device startup at power-up and power-down. The power supply monitor has built in hysteresis and filtering. This gives a high degree of immunity to false triggering due to noisy supplies.

In Figure 8, the trigger level is nominally set at 4 V. The tolerance on this trigger level is about ±5%. The power supply and decoupling for the part should be such that the ripple at AV_{DD} does not exceed 5 V ± 5% as specified for normal operation.

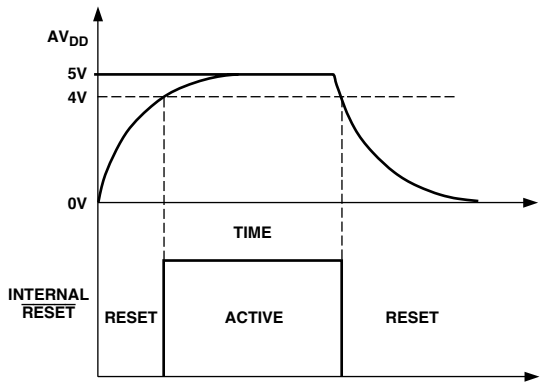


Figure 8. On-Chip Power Supply Monitor

HPF and Offset Effects

Figure 9 shows the effect of offsets on the real power calculation. An offset on Channel 1 and Channel 2 will contribute a dc component after multiplication. Since the dc component is extracted by the LPF, it will accumulate as real power. If not properly filtered, dc offsets will introduce error to the energy accumulation. This problem is easily avoided by enabling the HPF (i.e., Pin AC/$\overline{DC}$ is set logic high) in Channel 1. By removing the offset from at least one channel, no error component can be generated at dc by the multiplication. Error terms at cos(ωt) are removed by the LPF and the digital-to-frequency conversion (see Digital-to-Frequency Conversion section).

$$\left\{V\cos\left(\omega t\right)+\ V_{OS}\right\}\times\left\{I\cos\left(\omega t\right)+I_{OS}\right\}=$$

$$\frac{V\times I}{2}+V_{OS}\times I_{OS}+V_{OS}\times I\cos\left(\omega t\right)+I_{OS}\times V\cos\left(\omega t\right)$$

$$+\frac{V\times I}{2}\times\cos\left(2\omega t\right)$$

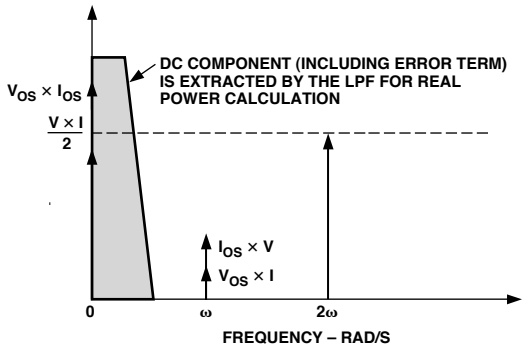


Figure 9. Effect of Channel Offset on the Real Power Calculation

The HPF in Channel 1 has an associated phase response that is compensated for on-chip. The phase compensation is activated when the HPF is enabled and is disabled when the HPF is not activated. Figures 10 and 11 show the phase error between channels with the compensation network activated. The ADE7755 is phase compensated up to 1 kHz as shown. This will ensure correct active harmonic power calculation even at low power factors.

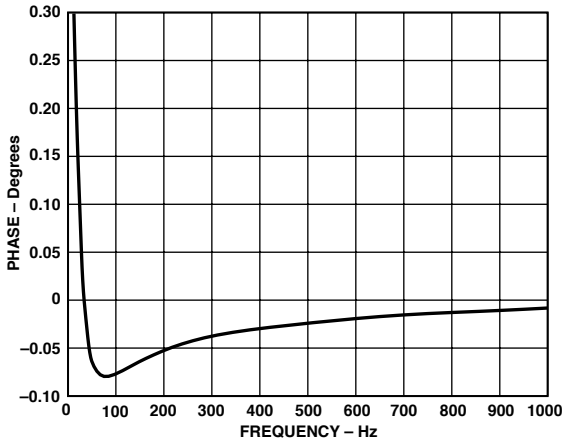


Figure 10. Phase Error between Channels (0 Hz to 1 kHz)

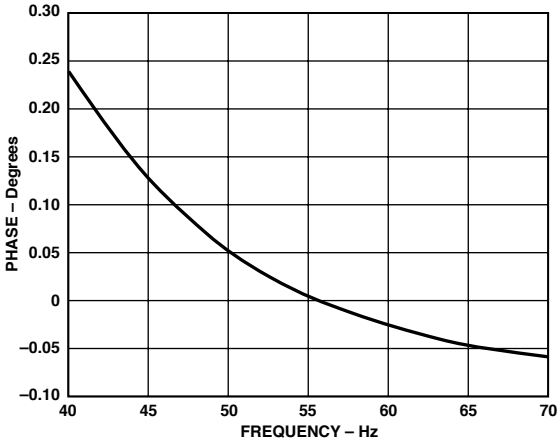


Figure 11. Phase Error between Channels (40 Hz to 70 Hz)

DIGITAL-TO-FREQUENCY CONVERSION

As previously described, the digital output of the low-pass filter after multiplication contains the real power information. However, since this LPF is not an ideal "brick wall" filter implementation, the output signal also contains attenuated components at the line frequency and its harmonics, i.e., cos(hωt) where h = 1, 2, 3, and so on.

The magnitude response of the filter is given by:

$$|H(f)| = \frac{1}{1+(f/8.9\ Hz)} \quad (5)$$

For a line frequency of 50 Hz this would give an attenuation of the 2ω (100 Hz) component of approximately –22 dBs. The dominating harmonic will be at twice the line frequency, i.e., cos (2 ωt), and this is due to the instantaneous power signal.

Figure 12 shows the instantaneous real power signal at the output of the CPF, which still contains a significant amount of instantaneous power information, i.e., cos (2 ωt). This signal is then passed to the digital-to-frequency converter where it is integrated (accumulated) over time to produce an output frequency. This accumulation of the signal will suppress or average out any non-dc components in the instantaneous real power signal. The average value of a sinusoidal signal is zero. Hence, the frequency generated by the ADE7755 is proportional to the average real power. Figure 12 shows the digital-to-frequency conversion for steady load conditions, i.e., constant voltage and current.

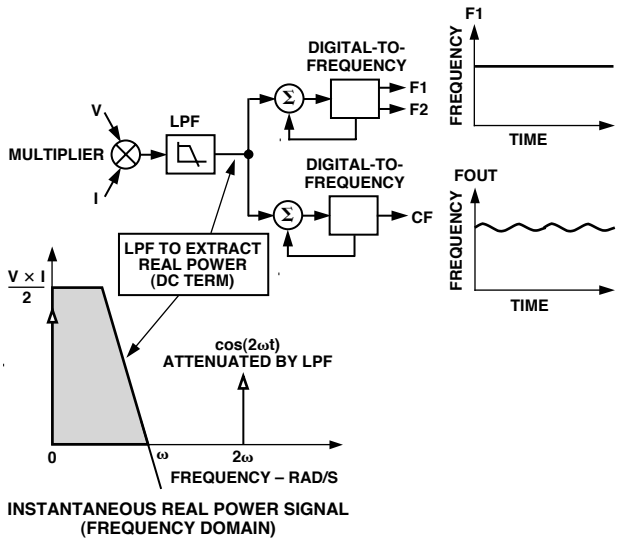


Figure 12. Real Power-to-Frequency Conversion

As can be seen in the diagram, the frequency output CF is seen to vary over time, even under steady load conditions. This frequency variation is primarily due to the cos (2 ωt) component in the instantaneous real power signal. The output frequency on CF can be up to 2048 times higher than the frequency on F1 and F2. This higher output frequency is generated by accumulating the instantaneous real power signal over a much shorter time while converting it to a frequency. This shorter accumulation period means less averaging of the cos (2 ωt) component. As a consequence, some of this instantaneous power signal passes through the digital-to-frequency conversion. This will not be a problem in the application. When CF is used for calibration purposes, the frequency should be averaged by the frequency counter. This will remove any ripple. If CF is measuring energy, e.g., in a microprocessor-based application, the CF output should also be averaged to calculate power. Because the outputs F1 and F2 operate at a much lower frequency, more averaging of the instantaneous real power signal is carried out. The result is a greatly attenuated sinusoidal content and a virtually ripple-free frequency output.

Interfacing the ADE7755 to a Microcontroller for Energy Measurement

The easiest way to interface the ADE7755 to a microcontroller is to use the CF high-frequency output with the output frequency scaling set to 2048 × F1, F2. This is done by setting SCF = 0 and S0 = S1 = 1 (see Table IV). With full-scale ac signals on the analog inputs, the output frequency on CF will be approximately 5.5 kHz. Figure 13 illustrates one scheme that could be used to digitize the output frequency and carry out the necessary averaging mentioned in the previous section.

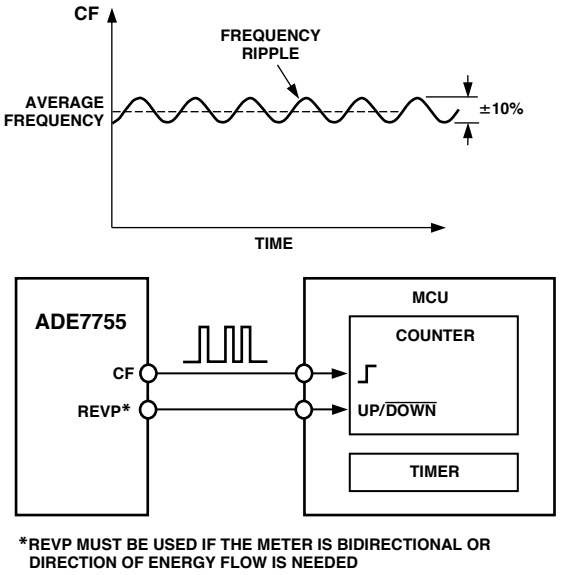


Figure 13. Interfacing the ADE7755 to an MCU

As shown, the frequency output CF is connected to an MCU counter or port. This will count the number of pulses in a given integration time that is determined by an MCU internal timer. The average power proportional to the average frequency is given by:

$$Average\ Frequency = Average\ Real\ Power = \frac{Counter}{Timer}$$

The energy consumed during an integration period is given by:

$$Energy = Average\ Power \times Time = \frac{Counter}{Time} \times Time = Counter$$

For the purpose of calibration, this integration time can be 10 to 20 seconds to accumulate enough pulses to ensure correct averaging of the frequency. In normal operation, the integration time can be reduced to one or two seconds depending, for example, on the required undate rate of a display. With shorter integration times on the MCU, the amount of energy in each update may still have some small amount of ripple, even under steady load conditions. However, over a minute or more, the measured energy will have no ripple.

Power Measurement Considerations

Calculating and displaying power information will always have some associated ripple that will depend on the integration period used in the MCU to determine average power and also the load. For example, at light loads, the output frequency may be 10 Hz. With an integration period of two seconds, only about 20 pulses will be counted. The possibility of missing one pulse always exists, since the ADE7755 output frequency is running asynchronously to the MCU timer. This would result in a one-in-twenty (or 5%) error in the power measurement.

TRANSFER FUNCTION

Frequency Outputs F1 and F2

The ADE7755 calculates the product of two voltage signals (on Channel 1 and Channel 2) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active low pulses. The pulse rate at these outputs is relatively low, e.g., 0.34 Hz maximum for ac signals with S0 = S1 = 0 (see Table III). This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation.

$$Freq = \frac{8.06 \times V1 \times V2 \times Gain \times F_{1-4}}{V_{REF}^{\ 2}}$$

where:

Freq = Output frequency on F1 and F2 *(Hz)*

$V1$ = Differential rms voltage signal on Channel 1 (Volts)

$V2$ = Differential rms voltage signal on Channel 2 (Volts)

Gain = 1, 2, 8, or 16, depending on the PGA gain selection made using logic inputs G0 and G1

V_{REF} = The reference voltage (2.5 V ± 8%) (Volts)

F_{1-4} = One of four possible frequencies selected by using the logic inputs S0 and S1—see Table II

Table II. F_{1-4} Frequency Selection

S1	S0	F_{1-4} (Hz)	XTAL/CLKIN*
0	0	1.7	3.579 MHz/2^{21}
0	1	3.4	3.579 MHz/2^{20}
1	0	6.8	3.579 MHz/2^{19}
1	1	13.6	3.579 MHz/2^{18}

NOTE

*F_{1-4} is a binary fraction of the master clock and therefore will vary if the specified CLKIN frequency is altered.

Example 1
Thus if full-scale differential dc voltages of +470 mV and –660 mV are applied to V1 and V2 respectively (470 mV is the maximum differential voltage that can be connected to Channel 1, and 660 mV is the maximum differential voltage that can be connected to Channel 2), the expected output frequency is calculated as follows:

Gain = 1, $G0 = G1 = 0$

F_{1-4} = 1.7 Hz, $S0 = S1 = 0$

V1 = +470 mV dc = 0.47 V (rms of dc = dc)

V2 = –660 mV dc = 0.66 V (rms of dc = |dc|)

V_{REF} = 2.5 V (nominal reference value)

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = \frac{8.06 \times 0.47 \times 0.66 \times 1 \times 1.7}{2.5^2} = 0.68$$

Example 2
In this example, with ac voltages of ±470 mV peak applied to V1 and ±660 mV peak applied to V2, the expected output frequency is calculated as follows:

Gain = 1, $G0 = G1 = 0$

F_{1-4} = 1.7 Hz, $S0 = S1 = 0$

V1 = rms of 470 mV peak ac = $0.47/\sqrt{2}$ volts

V2 = rms of 660 mV peak ac = $0.66/\sqrt{2}$ volts

V_{REF} = 2.5 V (nominal reference value)

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = \frac{8.06 \times 0.47 \times 0.66 \times 1 \times 1.7}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.34$$

As can be seen from these two example calculations, the maximum output frequency for ac inputs is always half of that for dc input signals. Table III shows a complete listing of all maximum output frequencies.

Table III. Maximum Output Frequency on F1 and F2

S1	S0	Max Frequency for DC Inputs (Hz)	Max Frequency for AC Inputs (Hz)
0	0	0.68	0.34
0	1	1.36	0.68
1	0	2.72	1.36
1	1	5.44	2.72

Frequency Output CF
The pulse output CF (Calibration Frequency) is intended for use during calibration. The output pulse rate on CF can be up to 2048 times the pulse rate on F1 and F2. The lower the F_{1-4} frequency selected, the higher the CF scaling (except for the high-frequency mode SCF = 0, S1 = S0 = 1). Table IV shows how the two frequencies are related, depending on the states of the logic inputs S0, S1, and SCF. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Hence, less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations (see Figure 2, signal processing block diagram).

Table IV. Maximum Output Frequency on CF

SCF	S1	S0	F_{1-4} (Hz)	CF Max for AC Signals (Hz)
1	0	0	1.7	128 × F1, F2 = 43.52
0	0	0	1.7	64 × F1, F2 = 21.76
1	0	1	3.4	64 × F1, F2 = 43.52
0	0	1	3.4	32 × F1, F2 = 21.76
1	1	0	6.8	32 × F1, F2 = 43.52
0	1	0	6.8	16 × F1, F2 = 21.76
1	1	1	13.6	16 × F1, F2 = 43.52
0	1	1	13.6	2048 × F1, F2 = 5.57 kHz

SELECTING A FREQUENCY FOR AN ENERGY METER APPLICATION
As shown in Table II, the user can select one of four frequencies. This frequency selection determines the maximum frequency on F1 and F2. These outputs are intended to be used to drive the energy register (electromechanical or other). Since only four different output frequencies can be selected, the available frequency selection has been optimized for a meter constant of 100 imp/kWhr with a maximum current of between 10 A and 120 A. Table V shows the output frequency for several maximum currents (I_{MAX}) with a line voltage of 220 V. In all cases the meter constant is 100 imp/kWhr.

Table V. F1 and F2 Frequency at 100 imp/kWhr

I_{MAX}	F1 and F2 (Hz)
12.5 A	0.076
25 A	0.153
40 A	0.244
60 A	0.367
80 A	0.489
120 A	0.733

The F_{1-4} frequencies allow complete coverage of this range of output frequencies on F1 and F2. When designing an energy meter, the nominal design voltage on Channel 2 (voltage) should be set to half scale to allow for calibration of the meter constant. The current channel should also be no more than half scale when the meter sees maximum load. This will allow over current signals and signals with high crest factors to be accommodated. Table VI shows the output frequency on F1 and F2 when both analog inputs are half scale. The frequencies listed in Table VI align very well with those listed in Table V for maximum load.

Table VI. F1 and F2 Frequency with Half-Scale AC Inputs

S1	S0	F_{1-4}	Frequency on F1 and F2 CH1 and CH2 Half-Scale AC Inputs
0	0	1.7	0.085 Hz
0	1	3.4	0.17 Hz
1	0	6.8	0.34 Hz
1	1	13.6	0.68 Hz

When selecting a suitable F_{1-4} frequency for a meter design, the frequency output at I_{MAX} (maximum load) with a meter constant of 100 imp/kWhr should be compared with Column 4 of Table VI. The frequency that is closest in Table VI will determine the best choice of frequency (F_{1-4}). For example, if a meter with a maximum current of 25 A is being designed, the output frequency on F1 and F2 with a meter constant of 100 imp/kWhr is 0.153 Hz at 25 A and 220 V (from Table V). Looking at Table VI, the closest frequency to 0.153 Hz in column four is 0.17 Hz. Therefore, F_2 (3.4 Hz—see Table II) is selected for this design.

Frequency Outputs

Figure 1 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low-frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating low going pulses. The pulsewidth (t_1) is set at 275 ms and the time between the falling edges of F1 and F2 (t_3) is approximately half the period of F1 (t_2). If, however, the period of F1 and F2 falls below 550 ms (1.81 Hz), the pulsewidth of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table III.

The high-frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90 ms-wide active high pulse (t_4) at a frequency proportional to active power. The CF output frequencies are given in Table IV. As in the case of F1 and F2, if the period of CF (t_5) falls below 180 ms, the CF pulsewidth is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulsewidth is 25 ms.

NOTE: When the high-frequency mode is selected, (i.e., SCF = 0, S1 = S0 = 1), the CF pulsewidth is fixed at 18 µs. Therefore, t_4 will always be 18 µs, regardless of the output frequency on CF.

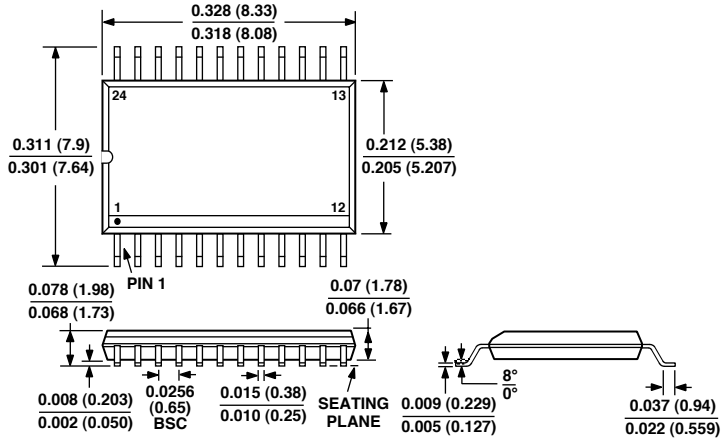
NO LOAD THRESHOLD

The ADE7755 also includes a "no load threshold" and "start-up current" feature that will eliminate any creep effects in the meter. The ADE7755 is designed to issue a minimum output frequency on all modes except when SCF = 0 and S1 = S0 = 1. The no-load detection threshold is disabled on this output mode to accommodate specialized application of the ADE7755. Any load generating a frequency lower than this minimum frequency will not cause a pulse to be issued on F1, F2, or CF. The minimum output frequency is given as 0.0014% of the full-scale output frequency for each of the F_{1-4} frequency selections (see Table II). For example, an energy meter with a meter constant of 100 imp/kWhr on F1 and F2 using F_2 (3.4 Hz), the maximum output frequency at F1 or F2 would be 0.0014% of 3.4 Hz or 4.76×10^{-5} Hz. This would be 3.05×10^{-3} Hz at CF ($64 \times$ F1 Hz). In this example, the no-load threshold is equivalent to 1.7 W of load or a start-up current of 8 mA at 220 V. IEC1036 states that the meter must start up with a load current equal to or less than 0.4% Ib. For a 5A (Ib) meter, 0.4% Ib is equivalent to 20mA. The start-up current of this design therefore satisfies the IEC requirement. As illustrated from this example, the choice of F1–F4 and the ratio of the stepper motor display will determine the start-up current.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

24-Lead Shrink Small Outline Package (RS-24)



C02897–0–5/02(0)

PRINTED IN U.S.A.